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D E C I S I O N
of 26 November 1999

Case Number: T 1060/97 - 3.5.2

Application Number: 92306317.6

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Title of invention:
Parabolic signal generator

Applicant:
Matsushita Electric Industrial Co., Ltd.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - denied"

Decisions cited:
-

Catchword:
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Boards of Appeal

Chambres de recours

Case Number: T 1060/97 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 26 November 1999

Appellant: Matsushita Electric Industrial Co., Ltd.
1006, Oaza Kadoma
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Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 23 May 1997
refusing European patent application
No. 92 306 317.6 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: A. G. Hagenbucher
C. Rennie-Smith

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division to refuse European patent application No. 92 306 317.6. The reason given for the refusal was that the subject-matter of claim 1 (main request) filed with the letter of 30 December 1996 and the subject-matter of claim 1 (auxiliary request) filed during oral proceedings on 24 April 1997 did not involve an inventive step.

II. The following prior art document was considered in the examining division's decision:

D1: Textbook: Halbleiter-Schaltungstechnik, U. Tietze & Ch. Schenk, Springer-Verlag 1983, pages 322 and 323.

III. Claim 1 of the main request is worded as follows:

"A parabolic signal generator including:

a sawtooth wave generation circuit (1) which, in response to a synchronization pulse signal applied thereto, is arranged to generate a sawtooth wave signal (2) having a centre point (A) which is crossed by a reference level;

an absolute value circuit (19) which can receive the sawtooth wave signal (2) from said sawtooth wave generation circuit (1) and is arranged to produce an absolute value signal (4) having a positive value relative to the reference level;

a logarithmic amplifier (20) which can receive the absolute value signal (4) from said absolute value circuit (19) and is arranged to produce a logarithmic output;

a linear amplifier (21) which can receive the logarithmic output from said logarithmic amplifier (20) and is arranged to produce a linear output; and

an anti-logarithmic amplifier (22) which can receive the linear output from said linear amplifier (21), and is arranged to produce an anti-logarithmic output,

characterised in that

the logarithmic output (Y_1) produced by said logarithmic amplifier (20) is defined as log of the absolute value signal (X) ($Y_1 = \log X$);

the linear output (Y_a) produced from said linear amplifier (21) is defined as the logarithm of the absolute value signal (X) to the power ($Y_a = \log X^{\acute{a}}$), \acute{a} being a parameter which can be altered by adjusting the gain of said linear amplifier (21);

the anti-logarithmic output (Y_o) produced from said anti-logarithmic amplifier (22) is defined as the \acute{a} th power of the absolute value signal (X) ($Y_o = X^{\acute{a}}$).

The single claim of the auxiliary request adds the following additional clause to the end of claim 1 of the main request:

"and wherein the absolute value circuit (19), said

logarithmic amplifier (20), said linear amplifier (21) and said anti-logarithmic amplifier (22) are respectively supplied with a common bias voltage (V_{ref}) which forms the reference level, the value of V_{ref} being set to a level which corresponds to the lowest level of the output signal of the absolute value circuit (19)."

IV. The appellant's arguments in the statement of grounds of appeal may be summarised as follows:

A significant aspect of the reasons for refusal of the application was based on the assumption that the reference voltage U_{ref} in D1 could be equated with the common bias voltage recited in the characterising part of the claim of the auxiliary request. Referring to three sketches filed with the grounds of appeal, showing the prior art according to D1 (sketches A and B) and the invention (sketch C), the appellant argued that the significant feature of the present invention (as defined according to the auxiliary request) was that the positive input terminal of the operational amplifiers and the base terminal of transistor T2 shown in sketch C all received a common bias voltage V_{ref} , whereas the corresponding terminals in the prior art were connected to ground as shown in sketch A. The bias voltage V_{ref} in the invention was not comparable with the voltage U_{ref} in the prior art, because that voltage was connected to the negative input of the first operational amplifier as shown in sketch A. The present invention offered the advantage that V_{ref} could be changed.

V. In a communication accompanying summons to oral

proceedings, the Board pointed out that there was no basis in the application as filed for sketch C and especially not for the arguments concerning the details of the connection of the common bias voltage. Contrary to the explanation in the grounds of appeal, sketch A represented the e-function generator shown in Figure 12.24 of D1, not a logarithmic amplifier, which was shown in Figure 12.22 on page 319 of the textbook cited as D1 (a copy of pages 318 to 323 of this book was enclosed with the summons). It was clear from the block diagram Figure 12.25 on page 323 of D1 that a reference voltage U_{ref} was required for the logarithmic (ln) and antilogarithmic (exp) amplifiers. If, following the example described on page 323 the same multifunction converter LH0094 was used for implementing the ln and exp functions in figure 12.25, the skilled person would normally use the same reference voltage for both converters, in order to avoid an unnecessarily large number of different reference voltages.

- VI. In the letter dated 3 November 1999, the appellant informed the Board that the appellant would not attend the oral proceedings and asked for a decision "based upon the documents lodged in relation to this application."

Reasons for the Decision

1. The appeal is admissible.
2. *Inventive step, main request*

2.1 As acknowledged in the present application, column 1, lines 3 to 34 of the published application, Figure 2 shows a conventional parabolic signal generator (DAF circuit for a large screen CRT) comprising a sawtooth wave generation circuit 1, which, in response to a synchronization pulse signal applied thereto, is arranged to generate a sawtooth wave signal 2 (shown in Figure 3A) having a centre point A which is crossed by a reference level V_{ref} . The sawtooth wave signal 2 is input into an absolute value circuit 3 which produces an absolute value signal 4 (shown in Figure 3B) having a positive value relative to the reference level. The output of the absolute value circuit is input into a circuit comprising resistors and diodes to produce a parabolic waveform.

2.2 As explained in column 1, lines 38 to 49 of the published application, the acknowledged circuit has the disadvantages that the parabolic waveform fluctuates due to the thermal characteristics of the diodes, and resistors and diodes must be changed when the focus characteristics or screen size of a CRT is altered. The subject-matter of claim 1 of the main request overcomes these disadvantages.

2.3 It is clear to the person skilled in the art that the disadvantages of the prior art circuit shown in Figure 2 of the present application arise from the use of resistors and diodes to produce the parabolic waveform. It is therefore obvious to look for an alternative to this circuit.

2.4 Document D1 is a well known textbook and discloses in chapter 12.7.3 on pages 322 and page 323 a parabolic

signal generator, shown in block diagram form in Figure 12.25, comprising a logarithmic amplifier producing a logarithmic output, a linear amplifier which receives the logarithmic output from said logarithmic amplifier and produces a linear output, and an antilogarithmic amplifier which receives the linear output from said linear amplifier and produces an antilogarithmic output.

2.5 It is obvious to the skilled person that such a parabolic signal generator does not suffer from the disadvantages mentioned in paragraph 2.2 above and, when connected to receive the output from the absolute value circuit 4 of the circuit shown in Figure 2 of the present application, will solve the problem underlying the present application.

2.6 When this is done, the logarithmic output (Y_1) from the logarithmic amplifier can be defined as log of the absolute value signal (X), that is $Y_1 = \log X$; the linear output (Y_a) produced from said linear amplifier can be defined as the logarithm of the absolute value signal (X) to the power \acute{a} , that is $Y_a = \log X^{\acute{a}}$, it being obvious to the skilled person that \acute{a} can be altered by adjusting the gain of said linear amplifier; and the antilogarithmic output (Y_o) from said antilogarithmic amplifier can be defined as the \acute{a} th power of the absolute value signal (X), that is $Y_o = X^{\acute{a}}$, this being mathematically equivalent to the relationship $y = x^{\acute{a}}$ given at the foot of page 322 of D1.

2.7 Thus, having regard to the prior art acknowledged in the present application and that known from D1, the subject-matter of claim 1 of the main request is

obvious to a person skilled in the art. It therefore does not involve an inventive step within the meaning of Article 56 EPC.

3. *Inventive step, auxiliary request*

3.1 As pointed out in the communication accompanying the summons to oral proceedings, there is no basis in the application as filed for sketch C. Neither the block diagram, Figure 1, nor the description of the present application reveals any precise details of the manner in which the common bias voltage is connected to the absolute value circuit 19, the logarithmic amplifier circuit 20, the linear amplifier 21, or to the antilogarithmic amplifier 22; it is only disclosed that the circuits 19, 20, 21 and 22 have reference input terminals supplied with a common bias voltage. The value of the bias voltage V_{ref} , or the fact that it may be changed, is not disclosed anywhere in the present application.

3.2 As may be seen from the block diagram Figure 12.25 on page 323 of D1 and from the more detailed circuit diagrams of temperature compensated logarithmic and antilogarithmic amplifiers, Figures 12.22 and 12.24 respectively, a reference voltage U_{ref} is required for the logarithmic and antilogarithmic amplifiers. If, following the example described on page 323 of D1, the multifunction converter LH0094 is used for implementing the logarithmic and antilogarithmic amplifiers shown in the block diagram Figure 12.25, the skilled person would normally use the same reference voltage for both these amplifiers and the linear amplifier, in order to avoid an unnecessarily large number of different

reference voltages. Since, as mentioned in the last paragraph of chapter 12.7.3 of D1, it is necessary for the input voltage received by the logarithmic amplifier to be positive (relative to the reference voltage of the logarithmic amplifier is meant), the reference voltage of the absolute value circuit cannot be less than the reference voltage of the logarithmic amplifier. Again, in order to avoid an unnecessarily large number of different reference voltages, it is obvious to the skilled person to use the same reference voltage for the absolute value circuit as for the three amplifiers.

- 3.3 The Board therefore concludes that the subject-matter of the claim according to the auxiliary request does not involve an inventive step within the meaning of Article 56 EPC, and, for that reason the request cannot be granted and the appeal must be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:

M. Kiehl

W. J. L. Wheeler