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D E C I S I O N
of 11 October 2002

Case Number: T 0500/98 - 3.4.3

Application Number: 90912955.3

Publication Number: 0450082

IPC: H01L 29/72

Language of the proceedings: EN

Title of invention:
Insulated gate bipolar transistor

Applicant:
DENSO CORPORATION

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (yes - after amendments)"

Decisions cited:
-

Catchword:
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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0500/98 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 11 October 2002

Appellant: DENSO CORPORATION
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Representative: Winter, Brandl, Fürniss, Hübner, Röss, Kaiser, Polte
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 17 February 1998 refusing European patent application No. 90 912 955.3 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: V. L. P. Frank
J. H. Van Moer

Summary of Facts and Submissions

I. The appeal lies against the decision of the Examining Division dated 17 February 1998 refusing the European patent application No. 90 912 955.3. The ground for the refusal was that claim 1 according to the main request contained subject-matter extending beyond the content of the application as filed (Article 123(2) EPC), and that the subject-matters of the claims of the first and second auxiliary request did not involve an inventive step having regard to the prior art documents:

D1: Patent Abstracts of Japan, vol. 12, No. 318 (E-650) [3165], 29 August 1988 & JP-A-63 81 861, and

D2: International Electron Devices Meeting, Technical Digest, December 6 to 9, 1987, Washington DC, US, pages 670 to 673

II. The appellant (applicant) lodged an appeal on 16 April 1998, paying the appeal fee the same day. The statement setting out the grounds of appeal was filed on 5 May 1998.

III. At the oral proceedings before the Board held on 10 October 2002 the appellant submitted an amended request based on claims 1 to 10, replacing all the previous requests.

IV. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the following patent application documents:

Claims: 1 to 10 submitted during the oral proceedings on 10 October 2002

Description: pages 1 to 10 filed with the statement of grounds of appeal on 5 May 1998
pages 11 to 30 as originally filed

Drawings: Figures 1 to 8 and 11 to 16 as originally filed
Figures 9 and 10 as filed on 16 August 1996

The wording of the only independent claim is as follows (emphasis added by the Board to show the amendments introduced in the course of the appeal proceedings with respect to the independent claim according to the first auxiliary request forming the basis of the above decision):

"1. An insulated gate bipolar transistor with a reverse conducting function, comprising:

[1] a first semiconductor layer (11) of a first conductivity type (p);

[2] a second semiconductor layer (12) of a second conductivity type (n) which is in contact with said first semiconductor layer (11);

[3] a first semiconductor region (13) of said first conductivity type (p) which is formed in said semiconductor layer (12) such that its junction portion terminates at the surface of said semiconductor layer (12);

[4] a second semiconductor region (14) of said second conductivity type (n) which is formed in said first semiconductor region (13) such that its junction portion terminates at the surface of said first semiconductor region (13);

[5] a gate electrode (33) formed on at least a channel region defined in the surface of said first semiconductor region (13) between said second semiconductor layer (12) and said second semiconductor region (14) with a gate insulating film (15) interposed therebetween;

[6] a first main electrode (31) whose contact portion is in contact with both said first semiconductor region (13) and said second semiconductor region (14);

[7] a second main electrode (22) for the supply of a main current through said first semiconductor layer (11)from said second to said first main electrode;

[8] a third semiconductor region (20) of said second conductivity type (n) which is electrically connected to said second main electrode (22) and formed in said second semiconductor layer (12), such that its junction portion terminates at the surface of said second semiconductor layer (12), so as to pass therethrough a reverse conducting current opposite in direction to the main current; and

[9] an embedded layer (23) of said second conductivity type (n) which is formed at or in the

vicinity of the interface (30) between said first semiconductor layer (11) and said second semiconductor layer (12), said embedded layer (23) having an impurity concentration higher than that of said second semiconductor layer (12);

[10] at least said first semiconductor region (13), said second semiconductor region (14) and said gate electrode (33) forming an element region (4);
characterized by

[11] at least one fourth semiconductor region (21) of said first conductivity type (p) located between said third semiconductor region (20) and said element region (4) in said semiconductor layer (12) such that its junction portion terminates at the surface of said second semiconductor layer (12) thereby ensuring a high withstand voltage; wherein

[9.1] said embedded layer (23) is provided below at least said element region (4) and said **fourth** semiconductor region (21) and is formed into a given pattern having openings through which charge carriers of the first and second conductivity type can pass whereby respective charge carriers can be injected from said first semiconductor layer (11) into said second semiconductor layer (12) and from said second semiconductor layer (12) into said first semiconductor layer (11); and wherein

[8.1] **said third semiconductor region (20) does not extend to said embedded layer (23)**."

V. In the decision under appeal the Examining Division concluded that although the claims of the first auxiliary request complied with the requirements of Articles 84 and 123(2) EPC, claim 1 of the request did not involve an inventive step for essentially the following reasons:

The insulated gate bipolar transistor (IGBT) according to claim 1 differs from the transistor disclosed in document D1 only in that:

(i) a fourth semiconductor region 21, acting as a guard ring, is located between the element region 4 and the third semiconductor region 20 for increasing the transistor's withstand voltage, and

(ii) the embedded layer 23 provided between the first and the second semiconductor layers (layers 11 and 12, respectively) has openings through which charge carriers can pass.

The objective technical problems solved having regard to these differences are, therefore:

(i) to improve the withstand voltage, and

(ii) to increase the on-current of the transistor disclosed in document D1.

However, feature (i), ie a field (or guard) ring, is disclosed in document D2 as improving the withstand voltage of an IGBT. A skilled person would, therefore, have used a field ring for achieving the same effect in the IGBT disclosed in document D1.

Moreover, the replacement in the IGBT disclosed in document D1 of the embedded layer's thinner portions by openings permits that the charge carriers traverse the embedded layer more easily and produces no other effects that would not have been foreseen by the skilled person: the on-resistance is lowered at the expense of the latch-up capability and the turn-off path resistance. Feature (ii) is, therefore, merely the result of balancing the advantages and disadvantages of a given measure, and does not involve an inventive step.

VI. The appellant argued essentially as follows in support of his request:

Document D1 discloses an IGBT with a continuous embedded layer formed by thicker and thinner portions which are electrically interconnected. To replace the thinner portions by openings is not an obvious modification, since such a replacement implies to modify the teaching of "forming" the thinner portions to "not-forming" them. Moreover, the removal of the thinner portions leaves the thicker portions as unconnected islands. The resulting structure, therefore, is no longer a conducting layer, and cannot reduce the transistor's turn-off time.

According to the application in suit, the embedded layer is not directly connected to the drain electrode via an n^+-type well region as in document D1 (cf. D1, Figure 1, well region 13), but constitutes a layer with improved conductivity. In document D1 the direct connection of the embedded layer to the drain electrode increases the transistor's on-resistance, due to a decrease of the amount of holes in the n-type

semiconducting layer. The embedded layer has thus a different function in the present application than in document D1.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

2.1 The Examining Division stated in the decision under appeal that there were no objections against the claims according to the first auxiliary request under Article 123(2) EPC, and the Board agrees with this finding.

2.2 In the course of the appeal proceedings the independent claim 1 has been amended with respect to the first auxiliary request before the Examining Division to specify that the third semiconductor region 20 does not extend to the embedded layer 23, ie feature [8.1] of this claim.

This feature was already implicitly disclosed by feature [8] of the claim which specifies that the third semiconductor region 20 is **formed in** the second semiconductor layer 12. In consequence, a portion of the second semiconductor layer 12 remains interposed between the third semiconductor region 20 and the embedded layer 23, and this region, therefore, does not extend down to the embedded layer. Moreover, feature [8.1] is disclosed in Figures 2, 3, 7, 8, 12 and 13 as originally filed.

2.3 Claim 1 was further amended in that in feature [9.1] the expression "said at least one semiconductor region (21)" was replaced by "said fourth semiconductor region (21)". This replacement is consistent which feature [11] of this claim in which the fourth semiconductor region (21) is defined.

2.4 The Board is, therefore, satisfied that these amendments fulfill the requirement of Article 123(2) EPC.

3. *Inventive step*

The only remaining issue is that of inventive step.

3.1 It is not in dispute that document D1 represents the closest state of the art.

This document discloses an IGBT having a reverse conducting function of low operating resistance built in it. The transistor comprises an embedded layer which is electrically connected to the transistor's drain electrode 10 through a n^+-type well region 13 which extends from the upper free surface of the device down to the embedded layer, a second drain electrode 14 and an external wire 18 connect this electrode to the drain electrode 10. The n^+-type embedded layer, which is in direct contact with the well region, is formed by thick and thin portions. The thin portions 12 are located directly under the n-type drain regions 16 of a current path of the transistor whereas the thick portions 11 are formed under the p-type base regions 4 (cf. D1, Abstract and Figure 1).

The presence of the embedded layer allows that the

operating resistance of the reverse conducting diode is low, since the reverse conducting current can flow through the highly doped embedded layer 11, 12 and the highly doped well region 13 to the transistor's drain electrode, ie through a low resistance path. The low reverse resistance leads in turn to a short turn-off time.

On the other hand, under forward bias condition, the charge carriers can pass more easily through the thinner portions 12 of the embedded layer than through the thicker portions 11. In consequence, the transistor's on-resistance is reduced with respect to a transistor in which the embedded layer is formed by a layer with a constant thickness.

The IGBT according to document D1 comprises thus an embedded layer allowing the passage of charge carriers under forward bias conditions and forming a low resistance path under reverse bias conditions.

3.2 The IGBT according to claim 1 differs from the IGBT disclosed in document D1 in that:

(i) a fourth semiconductor region (21), ie a guard ring, is located between the element region (4) and the third semiconductor region (20) to ensure a high withstand voltage (see above point IV, feature [11]);

(ii) the embedded layer (23) is formed into a given pattern having openings through which the charge carriers can pass (ibid, feature [9.1]); and

(iii) the third semiconductor region (20) does not

extend to the embedded layer (23) (ibid, feature [8.1]).

3.3 The provision of a guard ring, ie feature (i), improves the withstand voltage of the IGBT.

Moreover, according to the present application, the provision of openings in the embedded layer, ie feature (ii), permits the charge carriers to traverse this layer under forward bias conditions, as if the embedded layer were not provided (cf. column 8, lines 7 to 18 of the published application). In consequence, the transistor's turn-off time is reduced without degrading the efficiency of injection of the charge carriers from the first semiconductor layer 11 or increasing the transistor's on-resistance (cf. column 9, lines 7 to 14).

Furthermore, feature (iii) allows that the third semiconductor region 20 can be formed concurrently with the second semiconductor region 14, as it does not need to extend down to contact the embedded layer. This reduces the number of steps needed and simplifies the manufacturing process (cf. column 9, lines 15 to 16 and 27 to 29).

3.4 As regards feature (i) the Board agrees with the Examining Division that feature (i) was known from document D2 where a field ring structure is provided in an IGBT to improve the withstand voltage (cf. D2, page 670, right-hand column, lines 1 to 4 and Figure 1). Incorporation of feature (i) in the IGBT of document D1 was therefore merely the use of a known measure for its known purpose and was therefore obvious to a skilled person.

3.5 In the Board's view, however, the replacement of the thinner portions of the embedded layer by openings and the reduction in depth of the third semiconductor region so as not to contact the embedded layer are not obvious modifications of the transistor disclosed in document D1, since both features increase the value of the operating resistance of the reverse conducting diode and it is stated in this document that the embedded layer has to be connected to the drain electrode by means of a n^+-type well region. The provision of a continuous current path for the reverse conducting diode is, therefore, not merely a design option, but constitutes an essential aspect of the IGBT disclosed in this document.

Moreover, the fact that the embedded layer is not in direct electrical contact with the drain electrode through the third semiconductor region creates a different electric field structure within the transistor, since the embedded layer is left floating and is not held at the potential of the drain electrode as it is the case in the IGBT disclosed in document D1.

3.6 For the foregoing reasons, in the Board's judgement, the subject-matter of claim 1 involves an inventive step in the sense of Article 56 EPC and accordingly meets the requirements of Article 52(1) EPC.

The dependent claims concern further particular embodiments of the invention and are patentable for the same reasons.

Order

For these reasons it is decided:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the following documents:

Claims: 1 to 10 submitted during the oral proceedings on 10 October 2002

Description: pages 1 to 10 filed with the statement of grounds of appeal on 5 May 1998
pages 11 to 30 as originally filed

Drawings: Figures 1 to 8 and 11 to 16 as originally filed
Figures 9 and 10 as filed on 16 August 1996

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla