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D E C I S I O N
of 26 September 2002

Case Number: T 0320/99 - 3.4.3

Application Number: 91113424.5

Publication Number: 0471310

IPC: H01L 27/088

Language of the proceedings: EN

Title of invention:

MOS-type semiconductor integrated circuit device

Applicant:

NEC CORPORATION

Opponent:

-

Headword:

Auxiliary request/NEC

Relevant legal provisions:

EPC Art. 123(2), 52(1), R. 67

Keyword:

"Substantial procedural violation (yes) - allowable auxiliary request not considered"

"Reimbursement of appeal fee (no)- not equitable"

Decisions cited:

T 0004/98, T 0601/92, T 0821/96, T 0331/87, G 0010/93,

Catchword:

-



Case Number: T 0320/99 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 26 September 2002

Appellant: NEC CORPORATION
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Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 16 September 1998
refusing European patent application
No. 91 113 424.5 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: R. K. Shukla
Members: G. L. Eliasson
J. H. Van Moer

Summary of Facts and Submissions

I. European patent application No. 91 113 424.5 was refused in a decision of the examining division dated 16 September 1998. The ground for the refusal was that the subject matter of claims 1 to 3 according to the main request did not involve an inventive step having regard to the prior art documents

D1: Patent Abstracts of Japan, vol. 11, No. 41 (E-478) [2488] & JP-A-61-207 051; and

D3: US-A-4 657 628.

At the oral proceedings held on 3 March 1998 before the examining division, the applicant had submitted three auxiliary requests, of which the examining division did not admit first and second auxiliary requests into the proceedings in the exercise of its discretion under Rule 71(a) EPC, but had admitted the third auxiliary request.

Although the claims according to the third auxiliary request were considered to be allowable by the examining division, the application was refused, since it was understood that the applicant wanted an appealable decision on the basis of his main request.

II. The reasoning in the decision under appeal for refusing the main request can be summarized as follows:

The subject matter of claim 1 according to the main request does not involve an inventive step, since it would be obvious to provide silicide regions on the source/drain regions of the transistors known from

document D1 as taught in document D3. Due to the specific structure of the protective device of document D1, this would result in a silicide film on the drain region 3A of the first transistor which is spaced away from the gate electrode at a distance larger than that of the second transistor.

- III. The appellant (applicant) lodged an appeal on 26 November 1998, paying the appeal fee the same day. A statement of the grounds of appeal was filed on 12 January 1999 together with claims forming a main and a first auxiliary request. A further set of claims forming a second auxiliary request was filed with a letter dated 10 June 1999.

- IV. In response to a communication of the Board raising objections under Article 84 EPC against claim 1 of the main request, the appellant filed amended claims of the main request with the letter dated 8 August 2002.

- V. The appellant requests that the decision under appeal be set aside and a patent be granted according to one of the following requests:

Main request

Claims: 1 to 3 according to the main request filed with the letter dated 8 August 2002;

Description: pages 2, 8, 10, 11, 13 to 16, 19 to 25 as originally filed (pages 27 to 33 having been deleted), pages 1, 3, 3a, 4 to 7 filed with the letter dated 12 January 1995,

pages 9, 12, 17, 18, 26 filed with the letter dated 30 June 1995;

Drawings: Figures 1A to 6D as originally filed, Figures 7, 8A, 8B filed with the letter dated 30 June 1995.

First auxiliary request

Claims: 1 to 3 (part) according to the auxiliary request filed with the statement of the grounds of appeal, 3 (part) filed with the letter dated 23 April 1997;

Description and Drawings as for the main request.

Second auxiliary request

Claims: 1 to 3 filed with the letter dated 10 June 1999;

Description and Drawings as for the main request.

The appellant requested oral proceedings as a precaution against an adverse decision of the Board, and reimbursement of the appeal fee by reason of a substantial procedural violation.

VI. Claim 1 according to the main request under consideration reads as follows, where the differences with respect to the main request considered in the decision under appeal have been highlighted in bold type face:

"1. A semiconductor integrated circuit device

comprising a buffer circuit including a first MOSFET (121) to interface with an external device and an internal circuit operatively coupled to said buffer circuit and including a second MOSFET (122), said first MOSFET having a first gate electrode (106a) formed on a first gate insulating film (103), a first source region (113a, 107a) and a first drain region (113a, 107a) **being arranged such that there is no lateral offset between an edge of each of said source and drain regions (113a, 107a) and adjacent edge of said first gate electrode**, said second MOSFET having a second gate electrode (106b) formed on a second gate insulating film (103), a second source region (113b, 107b) and a second drain region (113b, 107b), said first MOSFET further having a first silicide film (112a) selectively formed on a surface of at least one of said first source and first drain regions at a first **lateral** distance from an edge of said first gate electrode, said second MOSFET further having a second silicide film (112b) selectively formed on a surface of at least one of said second source and second drain regions at a second **lateral** distance from an edge of said second gate electrode, said first distance being larger than said second distance."

Claims 2 to 3 are dependent claims.

VII. The appellant presented essentially the following arguments in support of his requests:

- (a) Silicide layers are widely used in MOS integrated circuits for reducing sheet resistance of the source/regions and thereby increasing the

operating speed of the device. It turns out, however, that the presence of silicide layers on the source/drain regions lowers the resistance against electrostatic discharge ("ESD resistance").

The problem addressed by the present invention relates to increasing the operating speed of an integrated circuit device without reducing the ESD resistance.

In view of the technical problem addressed by the present invention, the skilled person would not consider document D1, since it is not related to the use of silicide films. Furthermore, in the device of document D1, the drain is offset from the gate, whereas in the present invention, the silicide region in the drain is offset from the gate, but the drain is not offset from the gate.

- (b) At the end of the oral proceedings, the applicant had stated that he maintained both the main request and the auxiliary request. Since the examining division considered that the auxiliary request complied with the requirements of the EPC and was allowable, the correct course of action in accordance with the Legal advice 15/98 (OJ 1998, 113) was to issue a communication under Rule 51(4) EPC based on the auxiliary request. Since the applicant had not requested an appealable decision on the main request, the issue of the decision was a substantial procedural violation which justified the reimbursement of the appeal fee (cf. T 1105/96).

Reasons for the Decision

1. The appeal meets the requirements of Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

2. *Amendments and Clarity - Main Request*

2.1 With respect to claim 1 as filed, claim 1 according to the main request has been amended whereby: (i) the gate electrode does not specify that it includes at least a first metal; and (ii) the gate electrodes does not have spacers of an insulating film provided on their side faces. As replacement to feature (ii), claim 1 according to the main request specifies that the first source and drain regions are not offset from the first gate electrode, and first and second distances are designated as "first" and "second lateral distances" respectively in order to clarify the relation between the silicide films and the respective gate electrodes.

Claims 2 and 3 specify metal in the gate electrode (cf. feature (i) above).

2.2 In the decision under appeal, the examining division observed under "Further comments" that in order to lower the sheet resistance of the gate electrode, it was essential according to the application that the gate electrode included a metal.

The Board finds, however, that it is apparent from the application in suit that the use of a metal in a gate electrode is not indispensable in the light of the technical problem addressed by the invention, i.e. to increase the operating speed without reducing ESD resistance (cf. application as published, column 2,

lines 37 to 40). The use of metal (silicide) gates is common in the art and is not relevant to increasing the ESD resistance. Therefore, the skilled person would deduce from the application as filed that this feature was not relevant to the solution of the technical problem addressed by the present invention.

Furthermore, the use of a metal in a gate electrode is not explained as essential in the application as filed, and its removal does not require any modification of other features of the claimed device.

For the foregoing reasons, the omission of metal from the gate electrode does not go beyond the content of the application as filed (Article 123(2) EPC) (cf. T 331/87).

- 2.3 As to the replacement of feature (ii) with the specification that the first source and drain regions are not offset from the gate electrode, the Board is satisfied that this feature is supported by the application as filed, since it discloses two different embodiments for source/drain regions for the first transistor: One embodiment includes source-drain regions of lightly doped drain (LDD) type (Figures 1 to 4), and a second embodiment includes source/drain regions of the double diffused drain (DDD) type (Figure 5). In the second embodiment, both the lightly doped portion 107c and the heavily doped portion 113c of the source/drain regions are formed using the gate without any sidewall, i.e. a slight overlap exists between the gate and source/drain of the first transistor. Thus, the amendments as in feature (ii) also comply with the requirements of Article 123(2) EPC.

The claims are furthermore clear. Therefore, in the Board's judgement, the claims according to the main request meet the requirements of Articles 84 and 123(2) EPC.

3. *Inventive step - Main request*

3.1 The examining division considered that a device where the gate electrodes is not offset from the source and drain regions would not be obvious having regard to the prior art, since in document D1 there is necessarily such an offset. Therefore, a combination of the teaching of document D1 with that of document D3 would lead to a device having source and drain regions spaced away from the gate electrode (cf. the decision under appeal, "Further comments").

3.2 With respect to claim 1 forming the basis of the decision under appeal, present claim 1 according to the main request specifies that there is no lateral offset between an edge of each of the source and drain regions of the first MOSFET and adjacent edge of the first gate electrode. In other words, claim 1 according to the main request contains subject matter which was regarded by the examining division as involving an inventive step having regard to the cited prior art. The Board has no reason to reexamine on its own motion the examining division's finding on inventive step (cf. G 10/93, OF EPO 1995, 172, Reasons, item 4), so that the claim meets the requirements of inventive step (Article 52(1) EPC).

4. *Substantial Procedural Violation and Reimbursement of the Appeal Fee*

4.1 Under Rule 67 EPC, a reimbursement of the appeal fee is only possible if (a) the appeal is deemed allowable; and (b) the reimbursement is equitable by reason of a substantial procedural violation.

4.2 As regards the allegation of substantial procedural violation, it is evident from the minutes of the oral proceedings that

(i) in response to a question from the chairman whether the applicant wanted an appealable decision on the main request, the applicant's representative replied that he maintained his main and the auxiliary requests so that the applicant could decide the course of action (cf. the last paragraph of the Minutes); and

(ii) the applicant's above response was understood by the examining division to mean that the applicant wanted an appealable decision on the main request.

The applicant had not expressly requested a decision on the main request, and had maintained his allowable auxiliary request as well. Under these circumstances, the examining division had the obligation to consider the auxiliary request.

Consequently, the issue of the decision to refuse the application when an allowable auxiliary request was on the file was a substantial procedural violation.

4.3 The Board however finds that in the present case it would not be equitable to reimburse the appeal fee for the following reasons:

4.3.1 In the present case, the appellant has submitted with the statement of the grounds of appeal two set of claims according to a main request and a first auxiliary request. The main request filed with the statement of the grounds of appeal corresponds to a set of claims which was submitted at the oral proceedings before the examining division, but was not admitted under Rule 71(a) EPC. The appellant has not contested the refusal to admit this set of claims. The claims according to the first auxiliary request do not appear to have any correspondence to the claims submitted during the examination procedure. The second auxiliary request was filed later with the letter dated 10 June 1999 and corresponds to the auxiliary request which was considered allowable by the examining division.

4.3.2 Thus, regardless whether a substantial procedural violation occurred or not, the appellant requesting the grant of a patent on the basis of the main request had to appeal in order to obtain a reversal of the first instance decision on the issues of inventive step and clarity (cf. Minutes of the oral proceedings, page 2, first paragraph).

Under these circumstances, a reimbursement of the appeal fee is not equitable (cf. T 4/98, reasons, 13.3; T 601/92, reasons, 7.2 and 7.3; T 821/96, reasons, 2.3).

Therefore, the request for reimbursement of the appeal fee is rejected.

Order

For these reasons it is decided:

1. The decision under appeal is set aside.
2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the documents according to the main request as specified under item V above.
3. The request for reimbursement of the appeal fee is rejected.

The Registrar:

The Chairman:

P. Martorana

R. K. Shukla