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D E C I S I O N
of 18 March 2003

Case Number: T 0430/99 - 3.4.3

Application Number: 90104815.7

Publication Number: 0387836

IPC: H01L 27/06

Language of the proceedings: EN

Title of invention:
Semiconducor device for use in a hybrid LSI circuit

Applicant:
KABUSHIKI KAISHA TOSHIBA

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56, 111(1)

Keyword:
"Inventive step of the main and first auxiliary request (no)"
"Remittal for further prosecution on the basis of the second auxiliary request"
"Subject-matter submitted for the first time during the appeal proceedings.

Decisions cited:
-

Catchword:
-

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Case Number: T 0430/99 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 18 March 2003

Appellant: KABUSHIKI KAISHA TOSHIBA
72, Horikawa-cho
Saiwai-ku
Kawasaki-shi
Kanagawa-ken 210-8572 (JP)

Representative: Lehn, Werner, Dipl.-Ing.
Hoffmann Eitle
Patent- und Rechtsanwälte
Postfach 81 04 20
D-81904 München (DE)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 17 December 1998 refusing European patent application No. 90 104 815.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: V. L. P. Frank
M. B. Günzel

Summary of Facts and Submissions

I. European patent application No. 90 104 815.7 was refused by the decision of the Examining Division dated 17 December 1998 on the ground that the subject-matter of claim 1 did not involve an inventive step having regard to a combination of the prior art documents

D1: Patent Abstracts of Japan, vol. 11, No. 95 (E-492) (2542), 25 March 1987 & JP-A-61 245 563, and

D3: EP-A-0 110 313

II. The appellant (applicant) lodged an appeal on 12 February 1999, paying the appeal fee the same day. The statement setting out the grounds of appeal was filed on 15 April 1999 together with a new independent method claim 10 relating to the manufacturing method described in the application. Oral proceedings were requested as an auxiliary measure.

III. In a communication pursuant to Article 11(2) Rules of Procedure of the Boards of Appeal, annexed to the summons for oral proceedings, the Board informed the appellant of its provisional opinion that the subject-matter of independent device claim 1 did not involve an inventive step (Articles 52(1) and 56 EPC). It was further pointed out that the Board had limited itself to the patentability of the subject-matter of device claims 1 to 9, since the subject-matter of the independent method claim 10 was submitted for the first time in the appeal proceedings and had not been submitted for examination to the first instance.

IV. The appellant filed with his letter dated 18 February 2003 an amended main request and a first auxiliary request. Both requests contain independent device and method claims.

V. During the oral proceedings held on 18 March 2003 the appellant submitted a second auxiliary request consisting of a single method claim.

The appellant requested the reversal of the decision under appeal and the grant of a patent on the basis of one of the following requests:

Main request:
claims 1 and 10 as filed with the letter of 18 February 2003,
claims 2 to 9 as filed at the oral proceedings before the Examining Division on 26 November 1998.

First auxiliary request:
claims 1, 10 and 11 as filed with the letter of 18 February 2003,
claims 2 to 9 as for the main request.

Second auxiliary request:
claim 1 as filed during the oral proceedings.

VI. The independent claims according to these requests have the following wording:

Main request:

"1. A semiconductor device for use in a hybrid LSI circuit, comprising:

a) a semiconductor substrate (60; Fig. 4A) of a first conductivity type (P);

b) an epitaxial layer (Fig. 4B, 70) of a second conductivity type (N) provided on said substrate (60);

c) a first, second and third buried layer (Fig. 4D, 66) of the second conductivity type (N+) provided in a region located near an interface between said substrate (60) and said epitaxial layer (70), spaced apart from one another and having a higher impurity concentration (N+) than said epitaxial layer (70);

d) fourth buried layer regions (Fig. 4C, 4D; 68) of the first conductivity type (P+), provided in at least a first region between said first and second buried layers and a second region between said second and third buried layers, and having a higher impurity concentration (P+) than said substrate (60), both regions located near the interface between said substrate (60) and said epitaxial layer (70);

e1) a first well region (Fig. 4D, 72a) of the second conductivity type (N) provided in said epitaxial layer (70) on said first buried layer (66) and having an impurity concentration (N) higher than that of said epitaxial layer (70) and lower than that of said first buried layer (66);

e2) a second well region (Fig. 4D, 72a) of the second conductivity type (N) provided in said epitaxial layer (70) on said third buried layer (66) and having an impurity concentration (N) higher than that of said epitaxial layer (70) and lower than that of said third buried layer (66);

e3) a third well region (Fig. 4D, 74) of the first conductivity type (P) provided in said epitaxial layer (70) on said first region and said second region of said fourth buried layer (68) and having a lower impurity concentration (P) than said fourth buried layer (68);

f1) an insulated-gate FET (88, 90, 92) having a channel of the first conductivity type (P) provided in said first well region (72a) and using said first well region (72a) as a back gate;

f2) an insulated-gate FET (88, 96, 98) having a channel of the second conductivity type (N) provided in said third well region (74) and using said third well region (74) as a back gate;

g1) a first bipolar transistor (Fig. 4E-4G) provided on that region of said epitaxial layer (70) which is isolated by said third well region (74) from said first and second well regions (72a, 72b), and using that region of said epitaxial layer (70) as a collector having substantially the same impurity concentration throughout said epitaxial layer (70); and

g2) a second bipolar transistor (Fig. 4E-4G) provided in said second well region (72b) and using said second well region (72b) as a collector, and having an impurity concentration (N) higher than that of the collector (70) of said first bipolar transistor, and an impurity concentration profile identical to that of the first well region (72a)."

"10. A method for manufacturing a semiconductor device for use in a hybrid LSI circuit, comprising the following steps:

a) providing (Fig. 4A) a semiconductor substrate (60) of a first conductivity type (P);

b) forming (Fig. 4A) a first, second and third buried layer (66) of a second conductivity type (N+) spaced apart from each other in the surface of the substrate (60);

c) forming (Fig. 4B) fourth buried diffusion layers (68) of the first conductivity type (P+) and having a higher impurity concentration (P+) than said substrate (60) between said first and second and said second and third buried layers (66);

d) forming (Fig. 4C) an epitaxial layer (70) of the second conductivity type (N) on the surface of the substrate (60), said epitaxial layer (70) having a lower impurity concentration (N) than said first, second and third buried layers (N+);

e1) forming (Fig. 4D) a first resit layer on said epitaxial layer (70) and patterning said resist layer to form openings in said resist layer at positions corresponding to said first and third buried layers (66);

e2) forming (Fig. 4D) first and second well regions (72a, 72b) of the second conductivity type (N) in the epitaxial layer (70) through said openings above said first and third buried layers (66), said first and second well regions (72a, 72b) having an impurity concentration higher than that of said epitaxial layer (70) and lower than that of said first and third buried layer (66) respectively;

f1) removing said first resist layer and forming (Fig. 4D) a second resist layer on said epitaxial layer (70) and said first and second well regions (72a, 72b) and patterning said resist layer to form openings in said resist layer at positions corresponding to said fourth buried layers (68);

f2) forming (Fig. 4D) third well regions (74) of the first conductivity type (P) in the epitaxial layer (70) through said openings above said fourth buried layers (68), said third well regions (74) having an impurity concentration lower than that of the fourth buried layer (P+);

g1) forming (Fig. 4E-4G) a first insulated-gate FET (88, 90, 92) having a channel of the first conductivity type (P) in said first well region (72a) and using said first well region (72a) as a back gate;

g2) forming (Fig. 4E-4G) a second insulated-gate FET (88, 96, 98) having a channel of the second conductivity type (N) in said third well region (74) and using said third well region (74) as a back gate;

h1) forming (Fig. 4E-4G) a first bipolar transistor on a region of said epitaxial layer (70) above said second buried layer (66) which is isolated by said third well regions (74) from said first and second well regions (72a, 72b), said first bipolar transistor using that region of said epitaxial layer (70) as a collector having substantially the same impurity concentration throughout said epitaxial layer (70); and

h2) forming (Fig. 4E-4G) a second bipolar transistor in said second well region (72b) using said second well region (72b) as a collector and having an impurity concentration (N) higher than that of the collector (70) of said first bipolar transistor and an impurity concentration profile identical to that of the first well region (72a)."

First auxiliary request:

"1. A semiconductor device for use in a hybrid LSI circuit, comprising:

a) a semiconductor substrate (60) of a first conductivity type (P);

b) an epitaxial layer (70) of a second conductivity type (N) provided on said substrate (60);

c1) first to fifth buried layers (66, 68, 66, 68, 66) provided in a region located near an interface between said semiconductor substrate (60) and said epitaxial layer (70) and arranged, in a surface direction of said semiconductor substrate (60), adjacent to each other;

c2) said first, third and fifth buried layer (66) having said second conductivity type (N+) and a higher impurity concentration (N+) than said epitaxial layer (70); and

c3) said second and fourth buried layer (68) having said first conductivity type (P) and an impurity concentration (P+) higher than said semiconductor substrate (60);

d1) first to fifth well regions (72a, 74, 70, 74, 72b) respectively provided on said first to fifth buried layers (66, 68, 66, 68, 66);

d2) said first and fifth well regions (72a, 72b) being provided in said epitaxial layer (70) on said first and fifth buried layers (66), having said second conductivity type (N) with an impurity concentration (N) higher than that of said epitaxial layer (70) and lower than that of said first and fifth buried layer (66) and said first and fifth well regions (72a, 72b) having an identical impurity concentration profile;

d3) said second and fourth well regions (74) having said first conductivity type (P), being provided in said epitaxial layer (70) on said second and fourth buried layers (68) and having a lower impurity concentration (P) than said second and fourth buried layers (68); and

d4)* said third well region (70) being constituted by a region of said epitaxial layer (70) situated on said third buried layer (66) having substantially the same impurity concentration (N) throughout said region (70);

e1) a first insulated-gate FET (PMOS; 88, 90, 92) having a channel of the first conductivity type (P) provided in said first well region (72a) and using said first well region (72a) as a back gate;

e2) a second insulated-gate FET (NMOS; 88, 96, 98) having a channel of the second conductivity type (N) provided in said second well region (74) and using said second well region (74) as a back gate; and

f1) a first bipolar transistor (npn; 76, 94, 84) provided in said region of said epitaxial layer (70) situated on said third buried layer (66) and using that region of said epitaxial layer (70) as a collector; and

f2) a second bipolar transistor (npn; 76, 94, 84) provided in said fifth well region (72b) and using said fifth well region (72b) as a collector."

* This feature is specified as (d3) in the claim as filed and was amended to read (d4) by the Board.

The independent method claim 10 of this request is the same as for the main request.

Second auxiliary request:

The only claim of this request is the same as the independent method claim 10 according to the main or first auxiliary requests.

VII. The arguments of the appellant in favour of inventive step can be summarized as follows:

The four transistor structure (two bipolar transistors and two field effect transistors (FET)) disclosed in document D1 is different from the structure of the semiconductor device as claimed in the application in suit. Document D3 does not provide any motivation to alter this known structure in such a way as to arrive at the semiconductor device of claim 1. In particular, no reason is given in document D3 for providing a p-type well on a p^+-type buried layer on both sides of the structure shown in Fig. 9. Moreover, in document D3 the bipolar transistor is not formed within a region of the epitaxial layer having a constant impurity profile. Document D1 is also silent on the impurity

concentration profile of the epitaxial layer and, therefore, the skilled person would not be induced to employ an epitaxial layer having a constant impurity profile for forming a bipolar transistor even when the teachings of documents D1 and D3 are combined. The specific electrical conditions in the case when a bipolar transistor formed in an epitaxial well having a constant impurity profile is located at the side of the CMOS structure are very different from the electrical conditions when a diffused well region is used for forming the bipolar transistor. The specific arrangement of transistors chosen in the application is, however, very relevant for the interaction of the stacks in which the transistors of the semiconductor device are formed.

Furthermore, the semiconductor device disclosed in document D3 is closer to the semiconductor device according to the application, since in both devices the sequence of the transistors is the same: ie the p-channel metal oxide semiconductor FET (PMOS-FET) 62 is adjacent to the n-channel metal oxide semiconductor FET (NMOS-FET) 61 which is in turn adjacent to the npn bipolar transistor 70. However, document D3 does not give any indication as to where to form a further bipolar transistor.

Reasons for the Decision

1. The appeal is admissible.

2. *Main and first auxiliary requests*

2.1 Claim 1 according to the main request specifies that an insulated-gate FET (88, 96, 98, ie the NMOS FET) is formed in the third well region 74 (cf. feature f2 of

this claim). The third well region, however, is formed by two subregions, since it is provided on the first and second region of the fourth buried layer 68 (cf. ibid feature e3). The fourth buried layer's first region is located between the first and second buried layers and the second region is located between the second and third buried layers (cf. ibid feature d). It is, however, not specified in claim 1 according to this request in which one of the third well subregions the NMOS FET is formed. The claim embodies, therefore, two structures:

(i) a first structure in which the NMOS-FET and the PMOS-FET are adjacent to each other (cf. Fig. 4J of the application in suit included below), and

(ii) a second structure in which a bipolar transistor (I, II) is located between the two MOS-FETs.

Claim 1 of the first auxiliary request has been reworded to relate to the semiconductor device structure shown in Fig. 4J. It specifies a sequence of five buried layers which are adjacent to each other and on which the transistors are formed. This structure corresponds to the first structure of the main request.

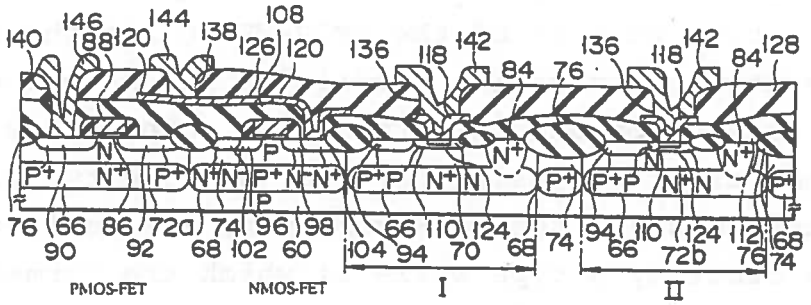

FIG. 4J

The discussion on inventive step in respect of claim 1 of the first auxiliary request, therefore, is applicable to claim 1 of the main request in so far as the claim concerns the first structure mentioned above.

The following discussion will, therefore, be based on claim 1 according to the first auxiliary request.

2.2 Document D1 discloses (cf. Fig. 1 of this document which is included below) a semiconductor device comprising a p-type substrate 11 on which a n-type epitaxial layer 13 is formed. Three n^+-type buried layers 12 are located at the interface between the substrate and the epitaxial layer (although in Fig. 1 the buried layer under the CMOS-FET is indicated as being n^--type it is clear from the figures showing the formation of the device that the three buried layers have the same doping level). On top of these n^+-type buried layers are formed respectively: (i) a first npn bipolar transistor A formed in the n-type epitaxial layer, (ii) a second npn bipolar transistor B formed in a n-type well 15 having a higher impurity concentration than that of the epitaxial layer and (iii) a complementary metal oxide semiconductor (CMOS) structure formed by a PMOS-FET C and a NMOS-FET D. The PMOS- and the NMOS-FET forming the CMOS structure are both formed on top of the same n^+-type buried layer 12. The n-type well 15 of the PMOS-FET C has the same impurity concentration profile as the n-type well 15 of the second npn bipolar transistor, since they are formed simultaneously (cf. Fig. 2). The two bipolar transistors and the CMOS structure are isolated from each other by p-type wells 14 which are formed into the epitaxial layer and are in contact with the p-type substrate. The first bipolar transistor A has a higher breakdown voltage than the second bipolar transistor B,

since the collector of transistor A is formed in the epitaxial layer which has a lower impurity concentration than the n-type well 15 in which the collector of transistor B is formed (cf. Abstract).

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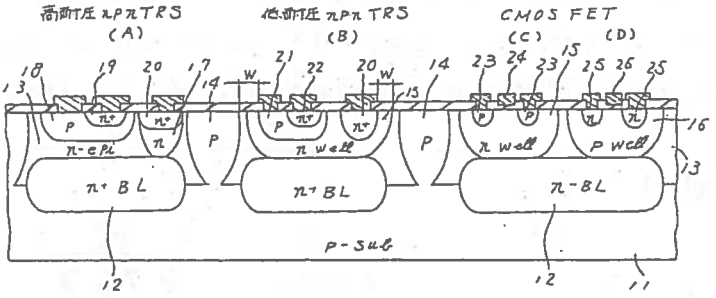


2.3 The semiconductor device according to claim 1 of the first auxiliary request differs, therefore, from the semiconductor device disclosed in document D1 in that:

(a) the NMOS-FET is formed within a p-type well overlying a p^+-type buried layer instead of a n^+-type buried layer as disclosed in document D1 (feature e2 of this claim);

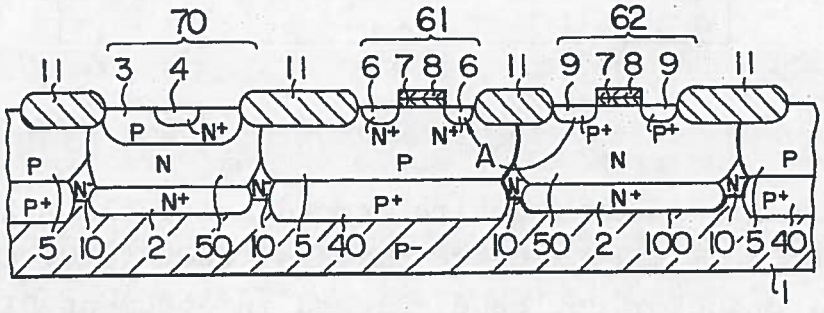
(b) a first bipolar transistor is adjacent to the NMOS-FET instead of being adjacent to the PMOS-FET as disclosed in document D1 (ibid feature f1);

(c) an isolation structure formed by p-type well overlying a p^+-type buried layer isolates the two bipolar transistors (ibid feature d3);

(d) the region of the epitaxial layer forming the collector of the first bipolar transistor has substantially the same impurity concentration throughout said region (ibid feature d4).

2.4 According to document D3 the provision of a p^+-type buried layer under the p-type well region of the NMOS-FET 61 connects electrically the p-type well 5 to the p-type substrate 1 via the p^+-type buried layer 40. This fixes the potential of the p-type well 5 of the NMOS-FET 61 and thus suppresses the expansion of the depletion layer around the n^+-type source and drain regions 6 (cf. D3, page 13, line 28 to page 14, line 7 and Fig. 9 of this document which is included below).

FIG. 9



Consequently, the technical effect achieved by the feature (a) mentioned above is to fix the electric potential of the NMOS-FET well region in the semiconductor device disclosed in document D1.

2.5 Document D3 discloses further that it has been proposed in the prior art to replace the p-type isolation wells, as used eg in the semiconductor device disclosed in document D1 (isolation wells 14), by a columnar structure comprising a p-type well overlying a p^+-type buried layer, since this replacement reduces the area of the isolation junctions formed by the p-type wells (cf. D3, page 3, lines 8 to 20 and page 4, lines 1 to 9 and lines 22 to 27).

Moreover, no separate isolation junctions are needed at all, if the n-type well regions 50 are located adjacent to the p-type well region 5. This arrangement of the wells further increases the integration density of the

semiconductor device (cf. D3, Fig. 9 and page 14, lines 22 to 27). This arrangement implies, in the case of using a p-type substrate, that the npn-bipolar transistor is located adjacent to the NMOS-FET instead of the PMOS-FET as disclosed in document D1. Since the well regions of the transistors are of the opposite conductivity type as the adjacent ones, no separate isolation structure is required.

In consequence, the technical effect achieved by features (b) and (c) mentioned in point 2.3 is to increase the integration density of the semiconductor device disclosed in document D1.

2.6 In the semiconductor device according to claim 1 the first bipolar transistor (element I in Fig. 4J) which has its collector formed by a region of the epitaxial layer is located adjacent to the CMOS-FET. This results, according to the appellant, in that the specific electrical conditions of the semiconductor device are improved, since the epitaxial layer 70 has a substantially constant impurity concentration. There is less disturbance between the NMOS-FET and the bipolar transistor, since the electric field distribution is more homogeneous in a region having a constant impurity concentration.

The technical effect achieved by feature (d) mentioned above in point 2.3 is to improve the specific electrical conditions of the semiconductor device disclosed in document D1.

2.7 The four features (a) to (d) differentiating the semiconductor device according to claim 1 from the semiconductor device disclosed in document D1 address, therefore, three technical problems, namely:

(i) to establish a well defined electric potential in the NMOS-FET well region (feature (a));

(ii) to increase the integration density (features (b) and (c)); and

(iii) to improve the device's specific electrical conditions (feature (d)).

It is the established case law of the Boards of Appeal that an aggregation of features exists when there is no functional interdependence between these features to achieve a technical effect over and above the sum of their respective individual effects, in contrast to what is assumed in the case of a combination of features (cf. Case Law of the Boards of Appeal, 4th edition 2001, I.D.6.4.2 'Partial problems').

In the present situation the Board considers that the three technical effects (i) to (iii) are not related to each other and are different partial problems that the skilled person would therefore address independently form each other.

2.8 As mentioned already under point 2.4, document D3 discloses that the provision of a p^+-type buried layer under the p-type well of the NMOS-FET maintains the electric potential of the well region at the substrate's potential.

The Board concludes, in consequence, that the provision of feature (a) in the semiconductor device disclosed in document D1 does not involve an inventive step having regard to the teaching of document D3.

2.9 Document D3 discloses further that no separate isolating structure is necessary when the npn bipolar transistor is located adjacent to the NMOS-FET (cf.

point 2.5). However, if a further npn bipolar transistor has to be formed in the semiconductor device, as it is the case for the device disclosed in document D1, an isolation structure is required, since no junction exists between two well regions having the same conductivity type. The skilled person learns from document D3 that the double well isolation structure (a p-type well overlying a p^+-type buried layer) allows a higher integration density than the p-type well 14 used for this purpose in document D1. For this reason, he would replace the first p-type well 14 (ie the one at the left-hand side of Fig. 1 of document D1) by a double well and would reverse the order of the elements of the CMOS-FET so that the NMOS-FET is adjacent to the npn bipolar transistor, rendering thus the second p-type well 14 redundant.

At the oral proceedings, the appellant argued that the combination of different embodiments of the same prior art was equivalent to the combination of different prior art documents. The conclusion that features (b) and (c) did not involve an inventive step was, therefore, based on a combination of three documents, namely document D1 and the embodiments disclosed in relation to figures 5 and 9 of document D3.

In the Board's view, however, it lies within the normal ability of a skilled person to choose, according to the particular circumstances he is faced with, the adequate measures from a document disclosing a plurality of measures directed to the same technical effect, in the present situation to increase the integration density.

For these reasons, the Board comes to the conclusion that features (b) and (c) do not involve an inventive step.

2.10 The Board concurs with the appellant in that the specific electric conditions and the interaction between adjacent stacks depend strongly on the impurity profiles of the wells forming the stacks. These effects, however, are discussed in the textbooks dealing with the physics of semiconductor devices and are, therefore, known by the skilled person designing these devices. The application in suit, moreover, is silent about any unexpected effect of the interaction between the stacks forming the NMOS-FET and the bipolar transistor formed in the epitaxial layer which goes beyond what is already known by the skilled person.

For the above reasons, the Board cannot recognize the presence of an inventive step in the use of an epitaxial layer having a constant impurity profile (ie feature (d)).

2.11 The appellant has contended that document D1 is not the closest prior art and argued that the structure of the semiconductor device disclosed in document D3 is closer to the device according to claim 1, since the sequence of PMOS-FET, NMOS-FET and bipolar transistor is the same. Consequently, the problem-solution approach should start from document D3 instead of document D1.

The Board, however, does not concur with the appellant on this point, since document D1 discloses a semiconductor device comprising four transistors. In particular, the impurity concentration of the well regions serving as collectors for the two npn bipolar transistors A and B are different and, therefore, the two bipolar transistors have different breakdown voltages and cutoff frequencies. In the Board's view, therefore, the semiconductor device disclosed in document D1 is closer to the structure and function of the device according to the application in suit than the device disclosed in document D3 (cf. column 4,

lines 22 to 41 of the published application). Document D1 is thus a state of the art that is closer to the application than document D3.

2.12 For the above reasons, it is the Board's judgement that the subject-matter of claim 1 according to the first auxiliary request does not involve an inventive step in the sense of Article 56 EPC.

As already discussed (cf. point 2.1) the above considerations are applicable to the subject-matter of claim 1 of the main request, so that claim 1 of the main request also does not involve an inventive step.

3. *Second auxiliary request*

The only claim of this request is directed to a method of manufacturing a semiconductor device for use in a hybrid LSI circuit. The subject-matter of this claim was submitted for the first time in the appeal proceedings and was not submitted for examination at the first instance. The manufacturing steps specified in the claim are based on the manufacturing method described in the application, but were never claimed in the originally filed application documents. It is, therefore, uncertain if the subject-matter of the claim was searched by the Search Division and if all the relevant documents are available for examination.

The Board has decided, for these reasons, to remit the case to the first instance pursuant to Article 111(1) EPC, second sentence, so that examination of this request in respect of the formal and substantive matters can take place. This gives the appellant the opportunity to have the case considered at two instances.

Order

For these reasons it is decided that:

The decision under appeal is set aside.

The case is remitted to the first instance for further prosecution on the basis of the claim of the second auxiliary request filed during the oral proceedings.

The Registrar: The Chairman:

N. Maslin R. K. Shukla