DECISION of 15 September 2005

Case Number: T 0492/02 - 3.5.1
Application Number: 96302771.9
Publication Number: 0738978
IPC: G06F 13/24
Language of the proceedings: EN

Title of invention:
Method and apparatus for interrupt communication in a packet-switched computer system

Applicant:
SUN MICROSYSTEMS, INC.

Opponent:
-

Headword:
Interrupt communication/SUN MICROSYSTEMS

Relevant legal provisions:
EPC Art. 56, 111(1)

Keyword:
"Inventive step over prior art cited in decision under appeal (yes)"
"Remittal to department of first instance for topping-up search"

Decisions cited:
-

Catchword:
-
DECISION
of the Technical Board of Appeal 3.5.1
of 15 September 2005

Appellant: SUN MICROSYSTEMS, INC.
2550 Garcia Avenue
Mountain View
CA 94043 (US)

Representative: Hogg, Jeffery Keith et al
Withers & Rogers LLP
Goldings House
2 Hays Lane
London SE1 2HW (GB)

Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 13 November 2001
refusing European application No. 96302771.9
pursuant to Article 97(1) EPC.

Composition of the Board:
Chairman: S. V. Steinbrener
Members: R. S. Wibergh
B. J. Schachenmann
Summary of Facts and Submissions

I. The appeal is against the decision of the examining division to refuse European patent application No. 96302771.9, published as EP-A-0 738 978.

II. The reason for the decision was that the subject-matter of independent claims 1 and 12 did not involve an inventive step having regard to the prior art documents D1: EP-A-0 644 489 and D3: US-A-5 319 753.

III. Together with the statement of grounds of 13 March 2002 the appellant filed a set of replacement claims 1-20. Reasons were put forward why the claimed subject-matter was regarded as inventive with respect to the prior art. It was requested to set aside the decision under appeal and grant a patent on the basis of the new claims.

IV. Independent claims 1 and 12 read as follows:

"1. A method of handling interrupt requests from a first device to at least one of a second device and a third device via a system controller coupled to each of the first, second and third devices, the second and third devices being interruptible devices, the second device including a first interrupt input queue and the third device including a second interrupt queue, each interrupt queue configured for accepting at least one interrupt request, the system controller being configured to store queue size information relating to
respective sizes of the first and second interrupt input queues, the method including the steps of:
(1) generating in the first device a first interrupt request with the second device as a destination device for said first interrupt request;
(2) receiving said first interrupt request at the system controller; and
(3) based at least in part on the queue size information, determining in the system controller whether the first interrupt input queue is full, and if not, then:
(3a) passing said first interrupt request to the second device; but if so, then:
(3b) sending the first device a signal indicating non-acknowledgement of said first interrupt request.

"12. An apparatus for handling interrupt requests from a first device to at least one of a second device and a third device via a system controller coupled to each of the first, second and third devices, the second and third devices being interruptible devices, the apparatus comprising: a first interrupt input queue at the second device and a second interrupt queue at the third device, each interrupt queue configured for accepting at least one interrupt request; and a system controller coupled to the first, second and third devices and configured to store queue size information relating to respective sizes of the first and second interrupt input queues of the second and third devices, and including a system controller input queue for receiving at least one interrupt request from the first device, a module for monitoring a number of interrupt requests present in each of the first and second interrupt queues of the second and third devices, and
logic configured to pass said interrupt request which is directed to the second device only if the first interrupt input queue is not full, the determination of whether the first interrupt input queue is full being based at least in part on the queue size information."

V. In a communication dated 10 January 2005, the Board indicated that it did not necessarily share the opinion of the examining division on the issue of obviousness with respect to D1 and D3. However, the subject-matter of the independent claims appeared to lack novelty over the document


D4, which claimed priority from US patent application 414 922 filed on 31 March 1995, constituted prior art according to Article 54(3),(4) EPC for all the contracting states designated in the present application. The Board, pointing out possible deficiencies in the application documents under Articles 84 and 78(1)(b) and Rules 27(1)(b) and 35(13) EPC as well, noted that a patent could not be granted on the basis of the present application documents but that the case might be remitted to the first instance for further prosecution without holding oral proceedings, which had been unconditionally requested by the appellant.

VI. In reply, the appellant replaced his previous unconditional request for oral proceedings by a request that oral proceedings should be appointed only if the Board intended to refuse the application, and observed
that the Board was in a position to set aside the decision and remit the case for further examination.

**Reasons for the Decision**

1. **Admissibility of the appeal**

   The appeal complies with the requirements referred to in Rule 65(1) EPC and is therefore admissible.

2. **The Invention**

   The present application relates to a system in which interrupt requests by electronic devices (e.g., processors) are centrally managed in a system controller. When a first device issues an interrupt request destined for a second (or third) device, the controller determines, on the basis of locally stored information about the size of the interrupt input queue in the destination device, whether this queue is full or not (box 475 in figure 3B; box 1530 in figure 10). Only if it is not full, i.e., if the destination device is in a position to handle the request, the system controller passes on the request. This centralised interrupt handling is said to provide for a flexible design which is easily scalable and adaptable to various sorts of devices (column 5, lines 45-53).

3. **Amendments**

   At the appeal stage one amendment has been made to claims 1 and 12. It is the addition of the feature that the second and third devices include the interrupt
input queues (as opposed to the queues being located in the central system controller). This addition is based on the initial application documents (see eg the "Slave Queues" depicted in figure 2) and thus satisfies Article 123(2) EPC.

4. The prior art

4.1 Document D1

D1, which the examining division regarded as the most relevant document, discloses a system comprising a plurality of processors communicating with a central interrupt controller which routes interrupt requests to an appropriate destination processor and queues them (see figures 3-5 and the associated text). The queuing order is largely determined by priority levels (page 5, lines 11-13). As shown in figure 6A (box 79), when the priority of an interrupt request to a processor is lower than or equal to the priorities of the interrupts already queued, the request is rejected and must be presented at a later time. The queues are in the controller, not in the destination processor. Their filling degree plays no significant role. Although the passage at page 5, lines 23-27, to which the examining division refers, mentions a depth of queue problem and overflow, it is in the Board's view too vague to be regarded as a sufficient disclosure of a rejection mechanism different from what is shown in figure 6A.

4.2 Document D3

D3 discloses an arrangement with two processors (10', 10'' in figure 1) which send interrupt request vectors
to each other via an interposed controller (900). The controller stores the vectors in predefined regions (970, 980 in figure 4) of a central memory (30’) and keeps track of the amount of information contained in each region of the memory using a queue counter (922, 926 in figure 3). If one of the processors desires to write an item into an interrupt queue it first has to detect whether the queue is full or not by comparing the queue counter with the queue size. If it is full, the interrupting processor will have to wait before it can store its request (column 5, lines 22-32). The aim is to prevent overflow (overwriting) of the central memory.

5. Inventive step

5.1 The examining division decided that the subject-matter of claims 1 and 12 (in the version then on file) did not involve an inventive step having regard to D1 and D3.

5.2 As noted above, D1 does not describe that the request queues are included in the destination devices, nor does it clearly disclose a request rejection mechanism which depends on the filling degree of a queue. The Board therefore considers that a skilled person, starting from this document, would not have recognised the need to store queue size information relating to the respective sizes of the interrupt request queues in the destination devices, as required by the claims. If anything, he would have been led to regard the priority of the request as the decisive criterion for passing or not passing the request. In the absence of a credible
technical problem, he would have had no reason to search for further prior art, such as D3.

5.3 As to D3, there is no controller which receives and passes requests but the processors do this themselves by means of the memory 900. Even if the skilled person had added such a controller to D3, for whatever reason, he would only have obtained a configuration in which the controller takes over the tasks of receiving and passing requests. But there would be no reason for locating the request queues in the processors, as now set out in the claims.

5.4 It follows that - contrary to the examining division's opinion - the subject-matter of claims 1 and 12 involves an inventive step (Article 56 EPC) with respect to a combination of documents D1 and D3.

6. Remittal to the department of first instance

Document D4 came to the Board's attention during the examination of the appeal. D4 is filed in the name of the appellant and, judging from its title and date of priority, is cited in the present application (as US application serial number 414 763 (sic), see column 4, lines 7-13). It is prior art according to Article 54(3),(4) EPC for all the contracting states designated in the present application and is prima facie so similar to the present application that it must be included in the novelty examination. Moreover, both the present application and D4 mention further related patent applications whose European counterparts could also turn out to be relevant. Since these documents have apparently not been considered by the
examining division the Board cannot accede to the appellant's initial request to grant a patent. In addition, the application documents appear to suffer from deficiencies of formal nature.

The appellant's observation in his last letter according to which he noted "that the Board is now in a position to set aside the decision and remit the case for further examination" is interpreted as a request for remittal of the case to the department of first instance, and in the present circumstances this appears indeed to be the best way to proceed. Hence, patentability of the claimed subject-matter should be re-examined in the light of the results of a topping-up search and the formal requirements should be taken into account.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance for further prosecution.

The Registrar:     The Chairman:

M. Kiehl      S. Steinbrener

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