Case Number: T 1486/12 - 3.5.02
Application Number: 08830942.2
Publication Number: 2181505
IPC: H03M 13/09, H04L 1/00
Language of the proceedings: EN
Title of invention:
Multi-layer cyclic redundancy check code in wireless communication system
Applicant:
Motorola Mobility LLC
Headword:
-
Relevant legal provisions:
EPC Art. 83
Keyword:
"Sufficiency of disclosure - yes (main request)"
"Remittal to first instance - yes"
Decisions cited:
-
Catchword:
-
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DECISION of the Technical Board of Appeal 3.5.02 of 16 October 2013

Appellant: Motorola Mobility LLC  
(Applicant)  
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Decision under appeal: Decision of the Examining Division of the European Patent Office posted 27 January 2012 refusing European patent application No. 08830942.2 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: M. Ruggiu  
Members: R. Lord  
P. Mühlens
Summary of Facts and Submissions

I. This is an appeal of the applicant against the decision of the examining division to refuse European patent application No. 08 830 942.2. The reason given for the refusal were that the application did not meet the requirement of Article 83 EPC.

II. In the statement of grounds of appeal dated 6 June 2012 the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the application documents according to the main request which formed the basis of the decision under appeal (i.e. based on claims 1 to 16 filed with letter dated 9 November 2011), or alternatively on the basis of one of the sets of claims also filed with the statement of grounds of appeal as first to fourth auxiliary requests. These remain the basis of the current requests. The appellant also requested reimbursement of the appeal fee.

III. In a communication accompanying a summons to oral proceedings, dated 29 July 2013 the board informed the appellant inter alia of its preliminary opinion that the application did meet the requirements of Article 83 EPC, but that the request for reimbursement of the appeal fee could not be granted, and that the board envisaged remitting the case to the department of first instance.

In a reply dated 29th August 2013 the appellant withdrew the request for reimbursement of the appeal fee and indicated that it agreed to the immediate
IV. Claim 1 of the appellant's main request reads as follows:

"A wireless communication device comprising:

a first Cyclic Redundancy Check, CRC, coder configured to generate a first block of CRC parity bits on a transport block, the first block of CRC parity bits based on a first generator polynomial, the first CRC coder attaching the first block of CRC parity bits to the transport block;

a segmenting entity having an input coupled to the first CRC coder, the segmenting entity configured to segment the transport block into multiple code blocks after attaching;

a second CRC coder configured to generate a second block of CRC parity bits on each code block, each of the second block of CRC parity bits based on a second generator polynomial, the second CRC coder attaching a second block of CRC parity bits to each code block, the second block of CRC parity bits attached to each code block is the second block of CRC parity bits generated based on the corresponding code block;

the second generator polynomial is different than the first generator polynomial and the first and second generator polynomials having a common degree;

a channel encoder configured to encode each of the code blocks including the attached second block of CRC parity bits."

Claim 9 of the appellant's main request reads as follows:
"A method in a wireless communication transmitter, the method comprising:

generating, at the transmitter, a first block of first Cyclic Redundancy Check, CRC, parity bits on a transport block, the first block of CRC parity bits based on a first generator polynomial;

attaching the first block of CRC parity bits to the transport block;

segmenting the transport block into multiple code blocks after attaching;

generating, at the transmitter, a second block of CRC parity bits on each code block, each of the second block of CRC parity bits based on a second generator polynomial, the second generator polynomial is different than the first generator polynomial and the first and second generator polynomials have a common degree;

attaching a second block of CRC parity bits to each code block, the second block of CRC parity bits attached to each code block is the second block of CRC parity bits generated based on the corresponding code block;

channel encoding, at the transmitter, each of the code blocks including the attached second block of CRC parity bits;

concatenating the code blocks after channel encoding."

Claim 10 of the appellant's main request reads as follows:

"A method in a wireless communication receiver, the method comprising:
removing, at the receiver, a second block of Cyclic Redundancy Check, CRC, parity bits attached to each of a plurality of received code blocks, the second block of CRC parity bits generated based on a second generator polynomial and based on the corresponding code block to which the second block of CRC parity bits are attached;

forming, at the receiver, an estimated transport block having a first block of CRC parity bits attached to the estimated transport block by concatenating the code blocks after removing the attached second block of CRC parity bits, wherein the first block of CRC parity bits attached to the transport block is based on a first generator polynomial that is different than the second generator polynomial, wherein the first and second generator polynomials have a common degree;

performing, at the receiver, a CRC check on the estimated transport block based on the first generator polynomial."

Claim 13 of the appellant's main request reads as follows:

"A method in a wireless communication transmitter, the method comprising:

generating, at the transmitter, a first block of Cyclic Redundancy Check, CRC, parity bits on a transport block, the first block of CRC parity bits generated based on a generator polynomial;

attaching the first block of CRC parity bits to the transport block;

interleaving the transport block after attaching;

segmenting the interleaved transport block into multiple code blocks;"
generating, at the transmitter, a second block of CRC parity bits on each code block, each of the second block of CRC parity bits generated based on the generator polynomial;

attaching a second block of CRC parity bits to each code block, the second block of CRC parity bits attached to each code block is the second block of CRC parity bits generated based on the corresponding code block;

channel encoding, at the transmitter, each of the code blocks including the attached second block of CRC parity bits;

concatenating the code blocks after channel encoding."

V. The appellant essentially argued as follows:

The interpretation of the claims relating to the functioning of the segmenting entity went beyond what was defined in those claims. The skilled person would have been able to put into effect the steps of "segmenting", "attaching" and "concatenating" defined in the claims, even though no specific hardware was disclosed in the application in this respect.

**Reasons for the Decision**

1. The appeal is admissible.

2. **Sufficiency of disclosure (Article 83 EPC) - Main request**

2.1 The board understands the decision under appeal as
being based on two aspects which the examining division considered did not meet the requirement of Article 83 EPC.

2.2 The first of these aspects is based on the interpretation by the examining division of independent claim 1 of the main request that the segmenting entity operates in such a manner that it must complete the operation of segmenting the transport block into multiple code blocks before the second CRC coder begins the operation of generation of a second block of CRC parity bits on each code block. Consequently, the division concluded that the application did not meet the requirement of Article 83 EPC, because of the absence in the application of any disclosure of how such a segmenting entity might be implemented in hardware. Similar objections were also raised in the decision under appeal with respect to the independent claims 9, 10 and 13, by reference to the arguments against claim 1.

2.2.1 Although the board agrees with the examining division that claim 1 requires that the segmenting entity is in some manner distinct from the second CRC coder, the board can see no reason to interpret the claim in such a manner that the operation of these two elements cannot overlap in time. In particular, the board considers that it is entirely consistent with the wording of the claim that the segmenting entity could generate a first code block and pass that code block to the second CRC coder, and that the second CRC coder could commence the operation of generating a second block of CRC parity bits for that first code block while the segmenting entity continues to generate
further code blocks. The board sees this interpretation as being consistent with what the examining division acknowledges to have been sufficiently disclosed. The board notes moreover that the skilled person would recognise that although the defined functions could be implemented in dedicated hardware, it would be equally possible to implement them by means of suitable programming of a general-purpose processor or of a DSP, and would therefore not consider it to be necessary to be able to identify a particular piece of hardware associated with each function.

2.2.2 As regards the question raised by the examining division of whether a skilled person would be able to carry out the subject-matter of the claims without undue burden, the board is of the view that a person who has studied digital signal processing at university level and who has acquired some experience in the field would undoubtedly be able, without substantial difficulty, to devise routines for segmenting strings of bits (i.e. data blocks), attaching (associating) parity bits to the segmented strings, and concatenating them, either as separate steps carried out on the whole string, or segment-wise. The board therefore considers that it can be assumed that the notional skilled person in this field is able to carry out the claimed entities or steps for segmenting, attaching and concatenating bit blocks without undue burden.

2.3 The second aspect of the reasoning of the decision under appeal concerns the argumentation in that decision that the independent claims required that the CRC parity bits be "physically attached" to the corresponding data block. The board can see no reason
for interpreting the claims in this manner, since this statement seems to the board to be meaningless in the context of such a device or method. In particular the board notes that neither the data nor the CRC parity bits have an independent physical existence, but are instead merely states in some form of electronic memory, so that physical attachment is not possible.

2.4 For the above reasons, the board concludes that the application in the form of the appellant's main request meets the requirement of Article 83 EPC relating to sufficiency of disclosure.

3. Since failure to meet the requirement of Article 83 EPC was the sole ground for refusal given in the decision under appeal, the board considers it to be appropriate to remit the case to the department of first instance so that the other requirements of the EPC can be addressed. It is therefore not necessary for the board to consider the appellant's auxiliary requests.
Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance for further prosecution.

The Registrar: 

The Chairman:

U. Bultmann 

M. Ruggiu