Case Number: T 0519/99 - 3.5.1
Application Number: 90103594.9
Publication Number: 0385317
IPC: H04N 5/93, H04N 7/32, H04N 9/64
Language of the proceedings: EN
Title of invention: Signal processing device
Patentee: CANON KABUSHIKI KAISHA
Opponent: Koninklijke Philips Electronics N.V.
Headword: Signal processing/CANON
Relevant legal provisions: EPC Art. 56, 123(2)
Keyword: "Inventive step - main request (no)"
"Admissibility of auxiliary request (no)"
Decisions cited: T 0401/02
Catchword: -
Case Number: T 0519/99 - 3.5.1

DECISION
of the Technical Board of Appeal 3.5.1
of 1 April 2004

Appellant: Koninklijke Philips Electronics N.V.
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Decision under appeal: Interlocutory decision of the Opposition
Division of the European Patent Office posted
25 February 1999 concerning maintenance of
European patent No. 0385317 in amended form.

Composition of the Board:
Chairman: S. V. Steinbrener
Members: W. E. Chandler
V. Di Cerbo
Summary of Facts and Submissions

I. This appeal is against the interlocutory decision of the opposition division concerning maintenance of European patent No. 0 385 317 in amended form. Opposition had been filed against the patent as a whole based on Article 100(a) EPC in conjunction with Article 56 EPC.

The opposition division held that claim 1 of the proprietor's main request did not involve an inventive step, but that the claims of the auxiliary request met the requirements of the EPC, having regard inter alia to following document:

D6: EP-A-0 204 578

II. Claim 1 of the allowed auxiliary request reads as follows:

"A data processing device comprising:

(a) encoding means (110) for encoding an information signal by utilizing correlation between components thereof to output encoded information having a compressed information content;

(b) a memory (104; 421; 22; 23) being used for write and read of the encoded information, said memory (104; 421; 22; 23) performing the read-out operation while performing the writing operation;

(c) decoding means (111) for decoding the encoded information read out from said memory (104; 421; 22; 23) to restore the information signal; and

(d) signal processing means (102) for effecting signal processing by simultaneously using the
information signal input into said encoding means (110) and the information signal output from said decoding means (111), wherein

said encoding means (110) includes a predictive differential encoding circuit (208; 413; 20),
timing control means (34) is provided for controlling the timing of resetting of write in said memory (22) and the timing of resetting of read from said memory (22), and

wherein said timing control means (34) controls first timing for resetting a predicting operation of said encoding means (20), second timing for resetting a write operation of said memory (22; 23), third timing for resetting a predicting operation of said decoding means (28) and fourth timing for resetting a read operation of said memory (22; 23), said first timing and said second timing being synchronized with each other, said third timing and said fourth timing being synchronized with each other."

III. The opponent (appellant) appealed the decision, and requested that the decision of the opposition division be set aside and that the patent be revoked. The respondent (proprietor) requested that the appeal be dismissed (main request). Both parties made an auxiliary request for oral proceedings.

IV. Following a communication from the Board containing an analysis of the issues to be discussed, the appellant filed additional evidence inter alia in the form of an extract from the book:

V. Oral proceedings were held on 1 April 2004 at which the respondent filed an auxiliary request comprising a set of amended claims, claim 1 of which was a combination of claims 1, 4 and 5 of the main request. At the end of the oral proceedings, the Board announced its decision to the parties.

VI. The appellant argued essentially as follows:

The distinguishing features of the encoding and decoding operation solved the "primary" objective technical problem of minimising the required memory capacity. The opposition division had already determined that the claimed solution to this was obvious.

The distinguishing features of resetting the predicting operations in synchronism with the resetting of the read and write operations of the memory solved the "secondary" problem of preventing error propagation, which followed as a direct consequence of using DPCM to solve the first.

The extract from the book by Jayant disclosed resetting the predicting operations periodically to zero, for example every $M^{th}$ line in image coding, to prevent error propagation in DPCM coding. Since in the prior art video processing circuit the read and write operations of the memory must also have been reset based on the line structure of the video signal, it followed automatically that the resetting operations were synchronised as claimed.
The auxiliary request should not be admitted. The communication accompanying the summons to the oral proceedings made it clear that the Board could have disregarded amendments that were not submitted in good time before the oral proceedings. The auxiliary request was filed during the oral proceedings. It should therefore be disregarded for lateness alone.

Moreover, although claim 1 of this request added only the subject-matter of claims 4 and 5 of the main request, it still raised further serious problems, notably under Article 123 EPC. Claim 1 of the main request concerned the embodiment (Figure 6/7 embodiment) in which the problem of error propagation was solved by synchronised resetting of the predictor and memory. The additional features of the auxiliary request related to a different embodiment (Figure 5 embodiment) that solved the same problem in a different way, namely by sending a synchronising code. However, these two embodiments had never been disclosed in combination. Moreover, the two embodiments were not compatible with each other. The patent application disclosed at column 6, lines 48 to 49 that the Figure 5 embodiment was "ineffective". This was why the Figure 6/7 embodiment was developed as an alternative, and the application stated at column 8, line 52 that it was "very effective". Furthermore, the originally filed application claimed these embodiments in different groups of claims, which were not dependent on each other.

VII. The respondent argued as follows:
To solve the "primary" problem of minimising the required memory capacity, the skilled person may have used an encoder and a decoder as known from D6. The other distinguishing features solved the objective technical problem of ensuring a stable operation of the whole data processing device.

D6 disclosed neither resetting the ADPCM predictor, nor resetting the read and write of the memory, nor the error propagation problem. Thus there was no hint to provide synchronisation between the prediction and the memory.

In general, it was not admissible to define additional problems, such as the appellant's "secondary" problem of the propagation of errors, and to invoke further documents in the inventive step argument.

In any case, even the three teachings of Figure 1 of the patent, D6 and the extract from the book on digital coding by Jayant did not lead to the subject-matter of claim 1. The extract from the book described that it was useful to reset predictor coefficients periodically to zero, but did not disclose or suggest the special synchronisation of resetting the prediction with other circuit operations. There were many other possible alternative synchronisations such as resetting in synchronism with other signals or on a time basis.

It was an additional indicator of patentability that despite being a leading company in this field, the opponent was not able to find a document showing the same or any similar synchronisation.

The auxiliary request was admittedly late, but it did not raise any undue difficulties because it merely involved the additional subject-matter of claims 4 and 5 of the main request.
Reasons for the Decision

1. The appeal complies with the requirements referred to in Rule 65(1) EPC and is, therefore, admissible.

2. Inventive step (main request)

2.1 The Board agrees essentially with the appellant's line of argument leading to the result that claim 1 of the main request does not involve an inventive step.

2.2 It is common ground that the closest prior art corresponds to that shown in Figure 1 of the patent in suit and discussed in the introductory part of the description. This discloses a general purpose video signal processing circuit structure that could be used, for example, for noise reduction. The circuit receives an input video signal and a signal delayed in a field memory and outputs a processed signal, which is also fed back to the field memory. The memory is controlled by a field memory control circuit synchronised to the video synchronisation signals.

2.3 The Board agrees with the appellant that this teaching also implicitly discloses timing control means for controlling the timing of resetting the writing and reading of the memory. This follows from the fact that, in the mentioned example of noise reduction, the video signal processing circuit needs some sort of synchronisation to keep track of corresponding parts of the video signal such as corresponding pixels on different lines or in different fields. This would have
to be effected by resetting the memory using the memory control circuit that is driven from the output of the sync separation circuit.

2.4 Claim 1 of the main request therefore differs from the prior art shown in Figure 1 by having:

(i) a predictive differential encoding circuit for encoding the signal written to the memory

(ii) decoding means for decoding the signal read from the memory

(iii) timing control means for resetting a predicting operation of the encoding means in synchronism with resetting a write operation of the memory

(iv) timing control means for resetting a predicting operation of the decoding means in synchronism with resetting a read operation of the memory.

2.5 It is common ground that the features of the predictive encoding and the decoding circuit (differences i and ii) can be considered to solve the problem of minimising the required memory capacity. This is what the appellant calls the "primary" problem.

2.6 The Board has no reason to question the opposition division's finding that it was obvious to encode and decode the signal to solve this problem in the light of the teaching of D6, which disclosed at page 6, lines 1 to 6 solving the same problem for any type of signal (see page 5, end of first paragraph) in an information
delay system by compressing (encoding) the signal before writing to the memory. Since D6 also discloses the use of predictive encoding (DPCM), this qualification is also obvious.

2.7 There was disagreement over the formulation of the problem that the appellant calls the "secondary" problem, namely the one deriving from synchronising the resetting of the predicting and the memory read and write operations (differences iii and iv). Since these features relate to the timing of the DPCM prediction, the "secondary" problem only becomes relevant once DPCM has been selected to reduce the memory requirement. Although there is thus some link between the two problems, the Board agrees with the appellant that the distinguishing features of the encoding and decoding operation and the resetting of the timing involve such different effects of the invention that there is no functional interdependence in the sense of a combination invention. Hence the Board judges that the appellant is correct in treating these features as relating to a classic case of solutions to independent partial problems, i.e. separately.

2.8 The Board judges that the solution to the "secondary" problem is also obvious even adopting the respondent's formulation of the problem as ensuring a stable operation of the whole data processing device. Firstly, stable operation is a universal goal of any circuit design and would be self-evident to the skilled person. Secondly, the Board agrees with the appellant that it is common knowledge that DPCM suffers from the problem of the propagation of errors. Moreover, it is apparent that the "extreme error propagation" mentioned in the
book on digital coding by Jayant, at page 335, second paragraph, indicates a problem of ensuring stable operation when DPCM is used in image coding applications.

2.9 Jayant discloses solving this problem by resetting the predictor coefficients periodically to zero, for example every $M^{\text{th}}$ line in image coding. The resetting of the predicting operation of the encoding would therefore be synchronised with the line structure of the video image. Since the resetting of the write operation of the memory is also synchronised with the line structure of the video image (see point 2.3, above), it follows that the two resetting operations are themselves in synchronism, as claimed.

Jayant also states that resetting the prediction is equivalent to restarting the decoding process, which implies that the resetting of the predicting operation of the decoding would also have to be in synchronism with the line structure of the video image and, hence, the resetting of the read operation of the memory, as claimed.

Even if there are other possibilities for resetting the predicting operations, the Board judges that the claimed ones are nevertheless obvious.

2.10 Accordingly, claim 1 of the main request does not involve an inventive step (Article 56 EPC).

3. Admissibility of auxiliary request

3.1 The Board judges that the circumstances of the present case are analogous to those in decision T 401/02 (Optisch variables Element/GIESECKE & DEVRIENT, not
published in OJ) from the present Board in a different composition. At point 5, the Board summarised the factors to be weighed up when exercising its discretion to admit late requests filed during the oral proceedings. These are:

(i) resulting delay in the procedure, including possible adjournment of the oral proceedings or remittal to the first instance. This could be the result of amendments that require more thorough examination (in that case under Articles 123(2) and 56 EPC)

(ii) whether the amendments are occasioned by any change in the facts of the case

(iii) whether the late filing is excusable owing to special circumstances.

In that case, it was not apparent that the amendments would be allowable under Articles 123(2) or 56 EPC, there had been no change in the facts of the case and the appellant gave no exceptional reasons that would have justified the late filing.

3.2 The Board judges that the circumstances of the present case are virtually the same. Concerning the delay in procedure of criterion (i), the Board agrees with the respondent that there are potential problems under Article 123(2) EPC when amalgamating the Figure 5 and 6/7 embodiments. In fact, a short discussion during the oral proceedings revealed that it was not even straightforward to determine whether claim 1 of the main request covered the
Figure 5 embodiment or not. Hence, neither the Board nor the appellant was in a position to assess the amendments on an ad hoc basis during the ongoing oral proceedings.

Concerning the change in case of criterion (ii), the Board judges that the extract from the book by Jayant filed by the appellant during the appeal represents evidence to support the alleged facts that the problems of error propagation and the solution of resetting the prediction operation in synchronism with the video signal were part of the skilled person's common general knowledge at the priority date. These facts had been asserted since the beginning of the appeal proceedings, at least, so that the Board judges that the facts of the case have remained essentially unchanged.

Concerning the special circumstances of criterion (iii), the appellant gave no exceptional reasons that would have justified the late filing.

3.3 For these reasons the Board does not admit the auxiliary request.

4. There being no other requests, it follows that the patent must be revoked.
Order

For these reasons it is decided that:

The decision under appeal is set aside and the patent is revoked.

The Registrar: The Chairman:

M. Kiehl S. Steinbrener